ABSTRACT OF THE DISCLOSURE

An apparatus and method for controlling CPU speed transition can use an SMI (System Management Interrupt) signal to perform speed transition of a CPU of a computer such as a notebook computer. However, if the bus master device is in the active state, a control operation needed for CPU speed transition is cancelled at the same time an event signal (e.g., a watchdog SMI or an embedded controller SMI) is created at prescribed intervals and the bus mater device active state is accordingly re-checked. Therefore, when the bus master device is in the active state, the control operation for CPU speed transition is cancelled to prevent the computer from hanging up, and the CPU speed transition control operation is periodically retried to increase a likelihood of a normal CPU speed transition or the normal CPU speed transition can be established.